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Manipulation of the Morphology of Semiconductor-Based Nanostructures from Core–Shell Nanoparticles to Nanocables: The Case of CdSe/SiO_2

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Abstract: The morphology of CdSe/SiO_2 was manipulated from core–shell-structured nanoparticles to nanocables by using a chemical vapor deposition (CVD) process. The growth of nanocables, with cores no more than 20 nm in diameter, is initiated by the formation of core–shell nanoparticles with SiO_2 as matrix and CdSe clusters dispersed inside. After the subsequent vaporization of the SiO_2 matrix, the follow-up CdSe vapor crystallizes with the remaining CdSe clusters as nuclei to form CdSe nanowires as the furnace was cooled to 1200 °C. During the controlled cooling of the furnace, the SiO vapor re-deposits to sheathe the nanowires. The thickness of the shell and the diameter of core were successfully controlled. The photoluminescence measurements show that the CdSe/SiO_2 nanocables have strong visible-light emission bands located at 590 and 688 nm, which are attributed to the defects induced by SiO_2 sheaths nanowires and the quantum confinement effect of the CdSe, respectively. The UV/Vis absorption spectra of the naked CdSe nanowires further validate the above-mentioned quantum confinement effect. The deterministic growth of these nanocables is very important for the design of the nanodevices based on them.

Keywords: cadmium selenide · core–shell nanoparticles · nanocables · nanostructures · optical properties

Introduction

Despite many studies that have focused on the relationship between particle size and optical behavior,[1] the control of the morphology, size, and surface chemistry of nanostructures is still a challenge to chemists. With the ongoing development of nanodevices, the preparation of nanocables, that is, semiconducting or metallic nanowires sheathed with an insulating shell, is of great significance.[2] To date, extensive attention has been paid to the encapsulation of semiconducting materials inside hollow cavities of silica nanotubes, which can then be used as sheaths to avoid the interference with the building blocks of a complex nanoscale circuit or to prevent oxidation of the semiconductor nanowires. In addition, semiconductor nanowires with a large refractive index, which are sheathed in silica shells are potentially applicable as optical waveguides. So far, several kinds of 1D nanocables based on semiconductors sheathed with a silica system have been achieved by employing a thermal evaporation method, such as germanium-filled silica nanotubes[3] and Si-silica nanocables,[2a] SiO_2-sheathed InS nanowires,[4] SiC-SiO_2-C coaxial nanocables,[5] and SiO_2-sheathed ZnS Nanowires.[6] In this context, Group II–VI semiconductors, such as ZnE and CdE (E = O, Se, Te), are believed to be of particular importance due to their unique optical, electrical, optoelectronic properties, and potential technological applications.[7] However, to date, few studies have been reported on the controlled synthesis of nanocables comprising these semiconductors.

With respect to CdSe/SiO_2 nanocables, despite the preparation of CdSe-filled sillica nanotubes by Geng et al.,[8] which are far too thick to actually use and were only prepared by a random growth route, the controlled preparation of much thinner CdSe/SiO_2 nanocables is in urgent demand, especially with regard to the control of the diameter of the CdSe inner and the thickness of the silica sheath.

In the meantime, conventional methods have proven successful for the fabrication of 1D nanostructures by either a vapor–liquid–solid (VLS) or a vapor–solid (VS) mechanism.[9] On the other hand, the growth process of nanocables is still poorly understood. Therefore, another of the goals of this work was to gain a better insight into the growth mech-

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anism of the nanocables, particularly with respect to the manipulation of the morphology from core–shell-structured nanoparticles to core-sheathed nanocables.

Herein, we report the control of the size of both the insulator SiO_2 shells and the semiconductor CdSe cores of the much finer CdSe/SiO_2 nanocables, in which the core is about 15 nm in diameter. These CdSe/SiO_2 nanocables were successfully obtained from CdSe/SiO_2 core-shell structured nanoparticles. Meanwhile, taking CdSe/SiO_2 composites as an example, we reveal a unique mechanism for the manipulation of the morphology from core–shell-structured nanoparticles to semiconductor nanowires sheathed by SiO_2. It is demonstrated that the CdSe/SiO_2 core–shell nanoparticles are formed first, followed by the evaporation of the SiO_2 sheath and growth of the remaining dispersive CdSe clusters in sequence. During the course of cooling the furnace, SiO_2 re-deposits on the nanowires to form the sheath. As a result, SiO_2-sheathed CdSe nanowires are formed. The mechanism of the manipulation of the morphology of CdSe/SiO_2 helps us to recognize the size control processes and morphology manipulation of the nanostructures. Furthermore, the unique mechanism of the formation of these nanocables pioneers a new approach for the controlled preparation of SiO_2-sheathed semiconductor nanowires. The deterministic growth of these nanocables is very important in the design of the nanodevices based on them.

Results and Discussion

Structural characterization: To explore the manipulation of the morphology of CdSe/SiO_2 nano-composites, samples were prepared by Methods 1–3, as described in the Experimental Section.

Figure 1a shows the scanning electron microscopy (SEM) image of the sample synthesized by Method 1. The resulting product comprises uniform nanospheres with a mean diameter of around 100 nm. The XRD pattern of the same sample (Figure 1b) confirms that the product includes the hexagonal CdSe phase and amorphous phase. Interestingly, the TEM image (Figure 1c) reveals that the nanospheres are core–shell-structured, that is there are brighter amorphous spheres with darker CdSe clusters of several nanometers in diameter dispersed inside. An EDX spectrum recorded for the nanospheres is shown in Figure 1d, and the result indicates that the nanospheres are composed of O, Si, Cd, and Se, and that the approximate atomic ratios of Si to O and Cd to Se are 1:2 and 1:1, respectively. This indicates that the amorphous phase is SiO_2. The extra Cu shown in the EDX spectrum stems from the Cu grid, and the C originates from the carbon film that is present on the Cu grid to improve the conductibility. The HRTEM image recorded for one of the particles (Figure 1e) reveals a structure of amorphous SiO_2 in which well-crystallized CdSe is dispersed inside. Amorphous rings in the SAED pattern also indicate the existence of the amorphous phase.

Figure 2a shows that the sample prepared according to Method 2 (see Experimental Section) comprises high-density 1D nanowire-like structures with typical lengths of up to tens of micrometers. The nanowires are rather uniform in their thickness. The XRD pattern of the product (Figure 2b) reveals that all diffraction peaks can be well indexed to the CdSe phase that is consistent with the standard data file (JCPDS No. 77-0046). The amorphous character, which is apparent at low angle, can be confirmed to originate from SiO_2 sheaths, as characterized by EDX later. TEM images allowed us to gain a better insight into the details of the products. The low-magnification TEM image of the wires is shown in Figure 2c. All the 1D nanostructures comprise core–sheath nanocable structures. The high-magnification TEM image reveals the obvious difference between the core and the shell (Figure 2e). The dark core corresponds to the CdSe crystal and the light sheath corresponds to amorphous SiO_2. Similarly, the EDX spectrum recorded for the wire (Figure 2d) confirms that the sample is composed of CdSe and SiO_2. The extra Cu and C (Figure 2d) originate from the same sources as mentioned above for the sample synthesized by Method 1.

All the above SEM and TEM observations suggest that the as-synthesized wire-like nanostructures have the characteristics of nanocable structures. The cores are 15–20 nm in diameter and the sheaths are 17–22 nm thick.

The detailed structure of the nanocable has been characterized by using HRTEM. The high-magnification HRTEM image corresponding to the high brightness pane in Figure 2e and the SAED pattern taken from the corresponding core are shown in Figure 2f. The clear core/sheath interface in the HRTEM image gives further evidence that the as-synthesized product is a nanocable. The SAED pattern taken along the $[2\bar{1}\bar{1}0]$ zone axis shows that the cores can be indexed as a hexagonal wurtzite phase with lattice constants of $a=0.429$ nm and $c=0.701$ nm. The spacing between the lattice planes perpendicular to the axis of the nanocable is about 0.701 nm, which corresponds to the distance between two (0001) planes of wurtzite-structured CdSe. The results suggest that the CdSe nanowires grow along the [0001] di-

Abstract in Chinese:

本文采用化学气相沉积法，使 CdSe/SiO_2 复合物直接从芯－壳结构的纳米颗粒转变为直径不大于 20 nm 的同轴纳米电缆。具体制备工艺如下：首先合成内部弥散着 CdSe 纳米团簇的 SiO_2 纳米球形颗粒；在随后的加热过程中，SiO_2 被还原为气态的 SiO 挥发，CdSe 纳米团簇沉积下来；在炉体温度重新冷却到 1200℃之前，后续输运过来的 CdSe 气体以这些纳米团簇为形核点生长形成纳米线；随后的冷却过程中，SiO 气体重新氧化成为 SiO_2 沉积下来，包覆在 CdSe 纳米线的表面形成壳层，最终形成 CdSe/SiO_2 纳米电缆。同时，绝缘体壳层的厚度和半导体芯部的直径成功地被控制。光致发光试验显示，CdSe/SiO_2 纳米电缆分别在 592 和 679 nm 两个波段产生很强的可见光发射，这分别归因于 SiO_2 包裹层引起的缺陷态和 CdSe 的量子限域效应。去除 SiO_2 壳层的 CdSe 纳米线的紫外－可见光吸收光谱进一步证明了验证了这种解释。这些纳米电缆确定性的合成对相关纳米器件的设计和组装非常重要。

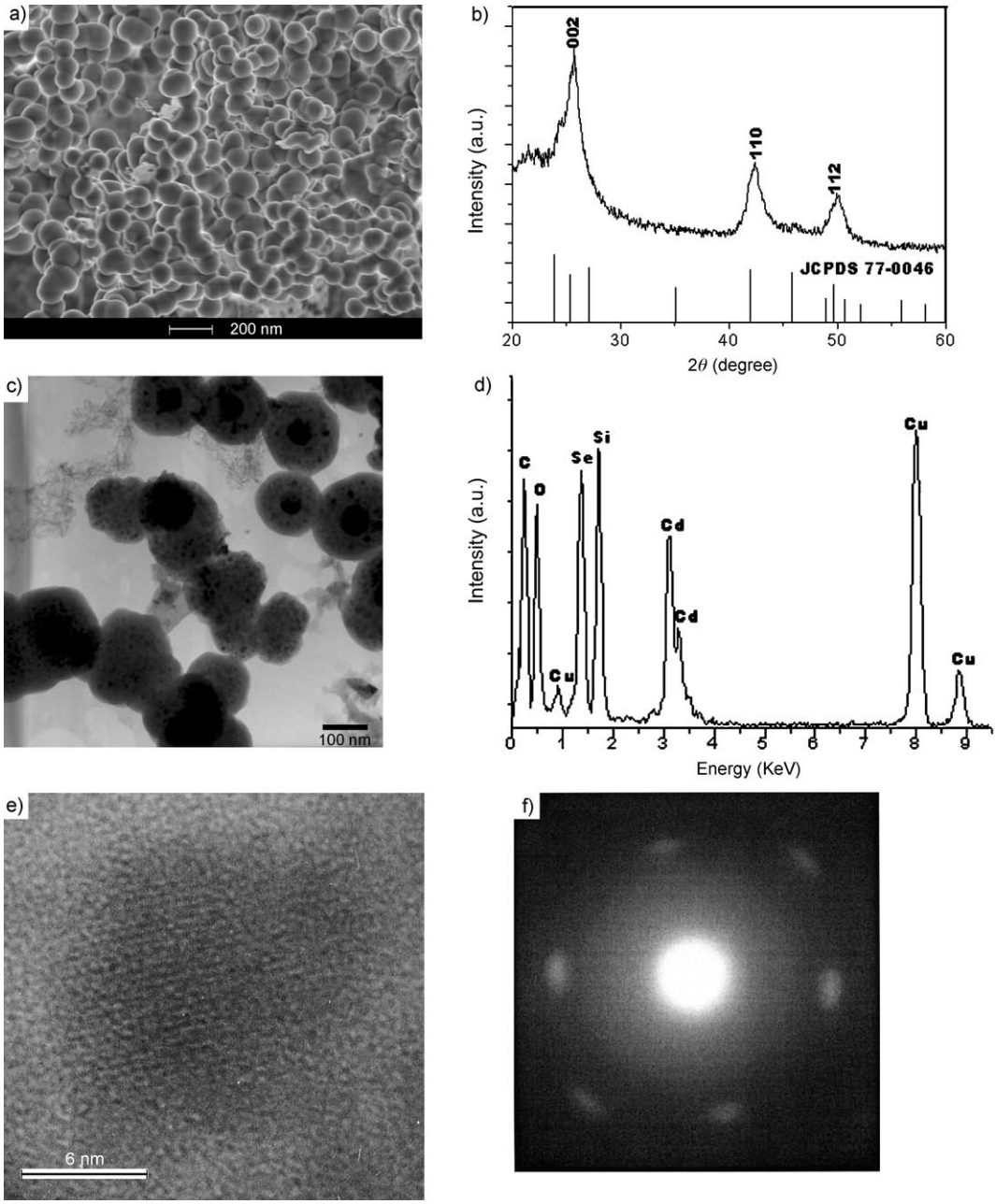

Figure 1. The morphologies, structures, and compositions of the sample prepared by Method 1 (see Experimental Section). a) SEM image of the sample; b) the corresponding XRD spectrum; c) TEM image of the nanoparticles; d) EDX spectrum recorded from one particle; e) high-resolution TEM image showing one of the CdSe clusters inside the particles. f) The corresponding electron diffraction pattern for the sample in (e).

rection and that that the nanocables are composed of a well-crystallized CdSe core surrounded by an amorphous silica sheath.

Figure 3a shows the TEM image of the tip of a nanocable prepared by Method 2. It can seen that the end of the nanocable is sheathed with the lighter amorphous phase with almost the same thickness as that on its side surface.

To further investigate the optical properties, we etched off the SiO_2 sheath by dipping the nanocables in a hydrofluoric acid (HF) solution (volumetric ratio of HF to H_2O is 1:10) for 24 h, and then dried the nanocables by flushing the system using de-ionized water. Figure 3b displays the TEM image of naked CdSe nanowires, and Figure 3b the corresponding HRTEM image. The core nanowires are around 15 nm in diameter.

Figure 4 shows the TEM images of four samples that for which the workup process was modified. The four samples were obtained as follows: the CdSe samples were synthesized by using Method 2, and thereafter the furnace temperature was kept at 1400 °C for 60 min. For the sample corresponding to Figure 4a, the electric source was switched off and the ceramic tube with the precursors and reaction prod-

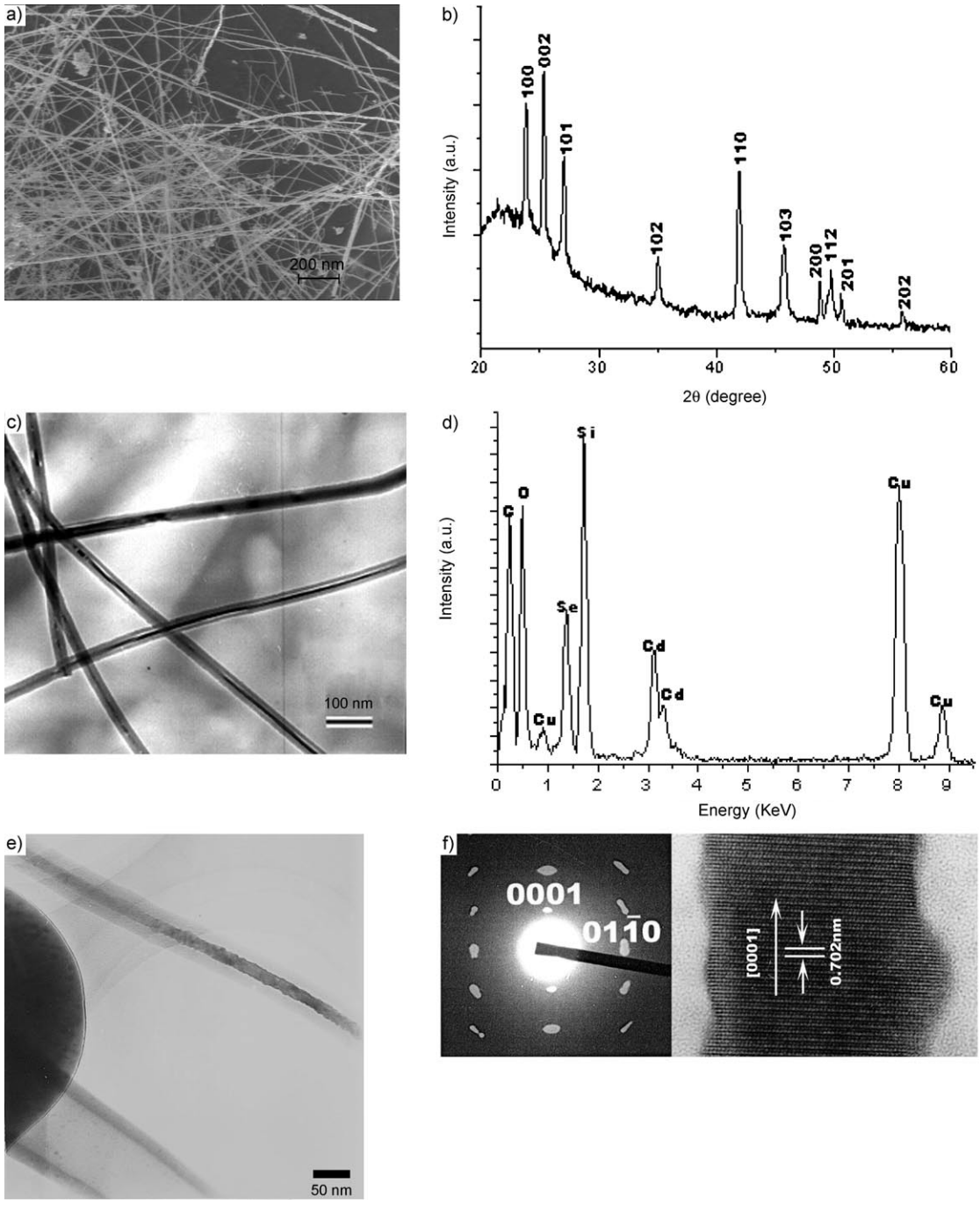

Figure 2. The morphologies, structures, and compositions of the samples prepared by Method 2 (see Experimental Section). a) SEM image of the sample; b) the corresponding XRD spectrum; c) the low-magnification TEM image of the nanocables; d) EDX spectrum recorded for one nanocable; e) the corresponding high-magnification TEM image of one of the nanocables; f) the HRTEM image and the SAED pattern corresponding to the high brightness pane of (e).

ucts was cooled in air; for the other three samples shown in Figures 4b–d, the time allocated for the furnace to be cooled to room temperature was 60, 90, and 120 min, respectively.

At room temperature, the four samples were taken out from the ceramic tube. It is clear that in the case of Figure 4a, the SiO_2 sheath is so thin that it can be neglected. In the case of Figure 4b, c, and d, the SiO_2 sheaths are 8, 27, and 66 nm, respectively, as listed in Table 1. Thus, the thickness of the sheath increases as a function of the cooling time.

Figure 5a and b are the SEM and TEM images, respectively, of one sample prepared by Method 3 (see Experimental Section). Figure 5b displays a coaxial nanocable morphology. According to our extensive examination, the brighter shell is amorphous SiO_2, and the darker core is

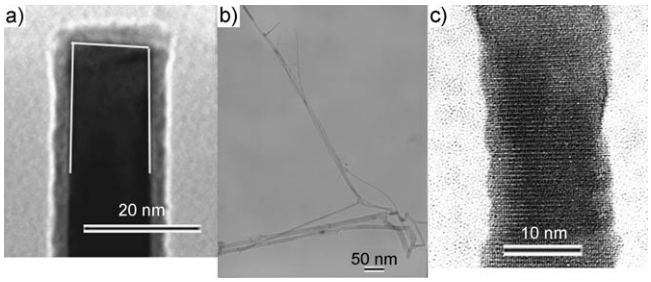

Figure 3. The TEM and HRTEM images of nanocables prepared by Method 2 (see Experimental Section). a) TEM image of the tip of a nanocable; b) TEM image of the naked CdSe cores, which were obtained by etching off the SiO_2 sheath using HF solution; c) the HRTEM image of the CdSe core.

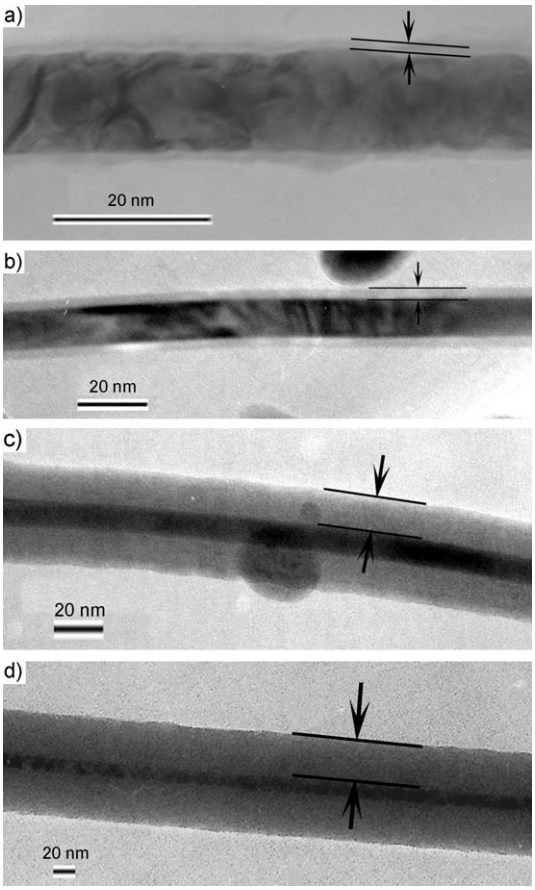

Figure 4. The TEM images of the $CdSe/SiO_2$ nanocables prepared by Method 2 (see Experimental Section). The morphology of the samples was dependent on the time allocated to allow the furnace to cool to room temperature: a) 0 (i.e. the ceramic tube with precursors and reaction products was cooled at air), b) 60, c) 90, and d) 120 min.

wurtzite-structured CdSe. As shown in the SEAD pattern, the CdSe core grows along the [0001] direction, which is the same as the sample shown in Figure 2b, except that the mean diameter is up to 300 nm.

Optical properties: The photoluminescence (PL) properties of the CdSe–SiO_2 nanocables prepared by Method 2 (see Experimental Section) were measured at room temperature, and the results are shown in Figure 6a. The nanocables have two emission bands centered at 590 nm and 668 nm, respectively. The rather intense peak at 668 nm observed in nanocables is similar to the reported emission band at about 668 nm in CdSe nanowires.[1d] This band is associated with the quantum confinement effect of the CdSe nanowires, and this assignment is not unreasonable since it is well known that silica is transparent with respect to visible light. Compared with the spectrum of silica nanotubes,[8] the lower peak at 590 nm observed in the as-synthesized nanocables may be attributed to the defects induced by the silica sheaths, such as oxygen vacancies.[4]

Table 1. Thickness of the shell as a function of the time allocated to the cooling process from 1400 °C to room temperature for samples prepared by Method 2.

Precursors	Si, Cd, and Se powders (with an atom ratio of 3:1:1.2)			
time of cooling[a] [min]	0 (Cooled in air)	60	90	120
thickness of the shell [nm]	0 (Neglected)	8	27	66

[a] From 1400 °C to room temperature.

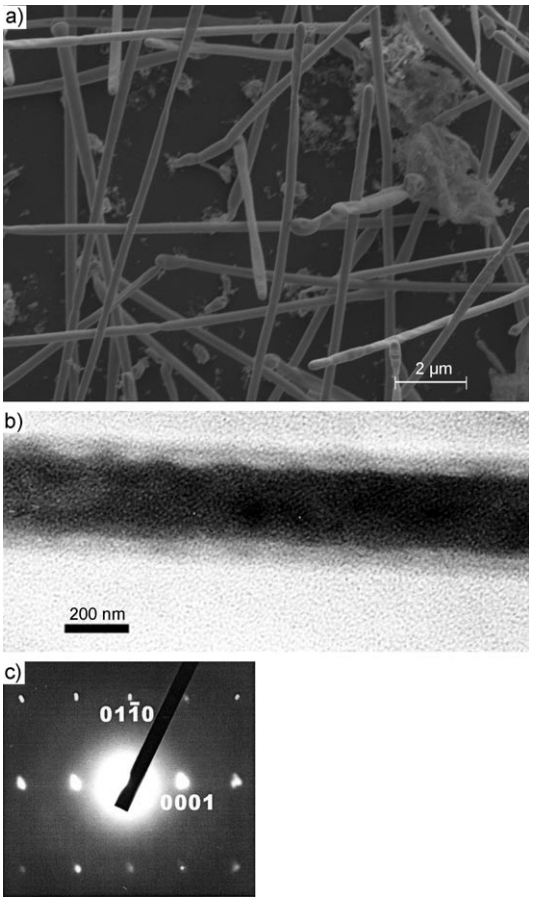

Figure 5. The SEM and TEM images and ED pattern of the samples prepared by Method 3 (see Experimental Section). a) SEM image of the sample; b) the corresponding TEM image; c) the corresponding ED pattern.

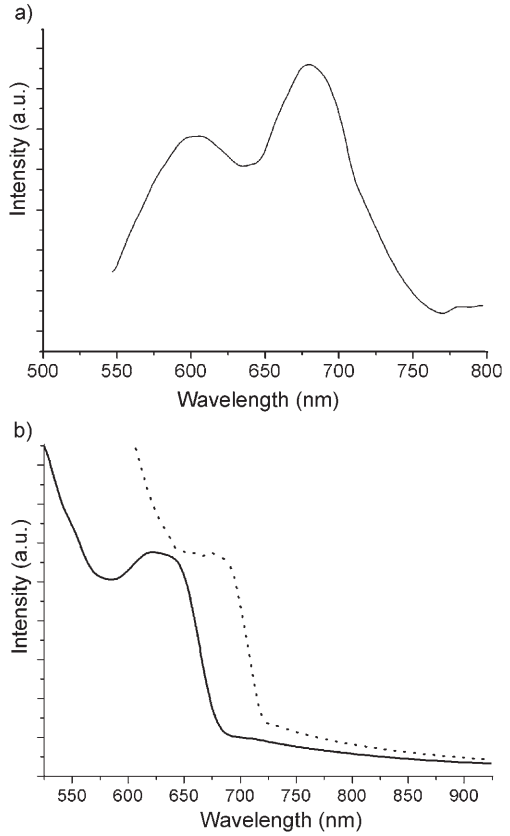

Figure 6. The photoluminescence and UV/Vis absorption spectra of the CdSe/SiO_2 nanocables. a) Room-temperature photoluminescence spectrum of the CdSe/SiO_2 nanocables prepared by Method 2; b) UV/Vis absorption spectra of the naked CdSe cores, which were obtained by etching off the SiO_2 sheath by using HF solution. The solid curve corresponds to the CdSe cores with a 15 nm diameter, the dashed curve to the CdSe cores with a 250 nm diameter, which correspond to the samples synthesized by Method 3 as shown in Figure 5.

The solid curve in Figure 6b shows the UV/Vis absorption spectrum of naked nanowire-like CdSe cores corresponding to those shown in Figure 3b. The CdSe nanowires display an absorption edge at about 680 nm, which corresponds to an electronic transition of a band gap of about 1.82 eV. There is a blue shift of 50 nm, 0.12 eV in energy, in comparison with that of bulk CdSe at 730 nm (1.7 eV), which might be attributed to the quantum confinement effect. In contrast, the dashed curve in Figure 6b displays the UV/Vis absorption spectrum of the naked CdSe cores corresponding to those shown in Figure 5 with a 250 nm diameter, which display an absorption edge at about 725 nm, nearly the same as that of bulk CdSe. This is because the sample is too big to exhibit the quantum confinement effect.

Manipulation mechanisms: In the following, the reasons for the changes in the morphology of CdSe/SiO_2 from core–shell-structured nanoparticles to coaxial nanocables, as well as the methods of size control, including manipulations of the diameter of CdSe nanowires and the thickness of the SiO_2 sheath, will be analyzed.

During preparation by Method 1, the gaseous Cd reacts with Se vapor to produce CdSe at 1200 °C. Meanwhile, the Si powder is oxidized to form SiO during heating by the oxygen in the ceramic tube. The CdSe nanoclusters nucleate from the vapor precursor on the Si substrate at about 950 °C. At the same time, the temperature of 950 °C corresponds to the decomposition temperature of SiO[2b,10] and indicates that SiO is the intermediate for the Si source. The SiO vapor is oxidized to form the solid SiO_2 phase and deposits together with the CdSe nanoclusters. As a result, SiO_2 particles embedded with CdSe clusters form. This is supported by our earlier work[11] and the experiments involving the preparation by Method 2 mentioned in the Experimental Section: 1) on the Si substrate at about 800 °C, only CdSe nanowires are formed assisted by Si.[11] 2) The CdSe/SiO_2 nanocables are produced on the Si substrate in the temperature zone above 950 °C during the preparation by Method 2.

For the preparation by Method 2, the CdSe/SiO_2 nanocable formation process is as follows: during heating the precursors from 1200 °C to 1400 °C, the temperature around the Si substrate is higher than 950 °C, and the solid-state SiO_2 reacts with Si to form SiO vapor. The SiO_2 decomposes and thus vaporizes. The subsequent CdSe nucleates with the remaining CdSe clusters as the nucleation sites. Accordingly, by the time that the furnace was cooled to 1200 °C, the CdSe nanowires with a longitudinal axis along the [0001] direction are formed on the silicon substrate, possibly by a vapor–solid mechanism.[10b] During the course of sequential cooling of the furnace, the SiO is re-oxidized to form the solid SiO_2 phase and deposits on the outer surfaces of the CdSe nanowires to form the sheath. Because the Cd and Se with designed dosage are used up before the furnace is cooled to 1200 °C, no CdSe nanoclusters are formed to embed in the SiO_2 shells. Consequently, CdSe/SiO_2 nanocables are grown.

In other work from our group,[6] SiO_2-sheathed ZnS semiconducting nanowires had been fabricated by the general thermal evaporation approach, in which there were sufficient data to demonstrate that the semiconducting core formed first and this was followed by the formation of the SiO_2 sheath in a synergic way by taking a ZnS/SiO_2 nanocable as an example. The growth of the ZnS nanowire and the silica sheath could be synergic, that is, the ZnS nanowire provides the template for the deposition of the silica sheath, and the silica sheath restricts the growth of ZnS along one dimension. What should be noted is that, for our work, the CdSe nanowires grow before the formation of silica sheath. If the growth of the CdSe nanowire and the silica sheath were synergic, SiO_2 would not seal the end of the CdSe nanowires, and the SiO_2 sheath on the end would be thinner than that on the side surface. However, Figure 4b clearly shows that the end of the SiO_2 sheath on the CdSe nanowire is almost the same thickness as that on the side surface. To validate our proposal, a series of samples were synthesized by Method 2 to which various rates of cooling were applied. According to Figure 4, the thickness of the SiO_2 sheath can be manipulated by altering the cooling rates after the

sample had been initially kept in the furnace at 1400 °C for 60 min. We found that as the rate of cooling increases, the thickness of the nanocables decreases. These observations provide further evidence that the growth of the SiO_2-sheathed CdSe nanowires occurs in sequence—first the CdSe nanowire and then the silica sheath. Thus, the thickness of the SiO_2 shell can be manipulated.

Furthermore, our resulting products prepared by the CVD route are much finer than those semiconducting nanocables synthesized by using a thermal evaporation method.[8] This might result from the much finer solid-state CdSe nuclei that arise due to co-deposition of SiO and CdSe during the time when the furnace temperature was kept at 1200 °C, the SiO_2 sheathes prevent the CdSe nanoclusters from growing larger. After the SiO_2 is vaporized off, a smaller nucleus will lead to a finer nanowire. This is why the diameter of the nanocables shown in Figure 5 is up to 300 nm. Moreover, the assistance function of Si powder observed in our earlier work[11] could be the reason why in this case the CdSe nanowires are not influenced by experimental parameters, such as the temperature and the gas flow rate. This is why our resulting products are uniform in shape and fine in size. In this way, the size of the CdSe cores can be controlled.

Conclusion

In summary, we have synthesized SiO_2/CdSe core-shell-structured nanoparticles and silica-sheathed CdSe semiconductor nanowires by a simple and general CVD approach. What is most important from this work is that we were able to manipulate the CdSe/SiO_2 composites from SiO_2 nanoparticles with CdSe nanoclusters dispersed inside to SiO_2-sheathed nanowires. Moreover, the size of the nanocables, including the diameter of the CdSe cores and the thickness of the SiO_2 sheath, can be controlled. We demonstrate that the growth of the nanocable structures follows a two-step process, namely, the formation of CdSe nanowires is followed by the deposition of the silica sheath. The results indicate that the CVD method is effective for the controlled fabricateion of SiO_2-sheathed semiconducting nanowires. This approach has allowed us to further investigate the controllable growth mechanism of the CdSe/SiO_2 nanocables through the suitable manipulation of synthetic parameters. The intense emission bands at 592 nm and 668 nm were detected in the as-synthesized CdSe/SiO_2 nanocables. The UV/Vis absorption spectrum shows that the naked nanowire-like CdSe cores display an absorption edge at about 680 nm. The final products could be used in the fields of nanoelectronics and photonics.

Experimental Section

The growth of CdSe/SiO_2 nanocables was carried out in a horizontal-tube furnace by employing a simple CVD process. Experimentally, an alumina tube was mounted horizontally inside a high-temperature furnace. The Si powder and a mixture of the pure Cd (99.999 %) powder and the pure Se (99.999 %) powder (atom ratio 1:1.2), which were used as precursors, were loaded in ceramic boats and placed in the middle of the furnace. The Si wafer was located 6 cm downstream of the precursor powders. The tube was then sealed. After the system had been flushed with high purity argon for 1 h, a constant flow of 1 atm high purity Ar gas (60 sccm) was passed through the system. This acted as a carrier gas to transport the sublimated vapor to cooler regions within the tube furnace for deposition. The samples were synthesized by using three different methods.

Method 1: The powders were heated to 1200 °C at a rate of 120 °C min^{-1} and held at this temperature for 60 min before the furnace was cooled to room temperature at a rate of 20 °C min^{-1}.

Method 2: The powders were heated to 1200 °C at a rate of 120 °C min^{-1} and held at this temperature for 60 min. Then the temperature was increased to 1400 °C over 3 min and held at this temperature for 60 min, after which the Cd and Se with designed dosage were exhausted. The furnace was then cooled to room temperature at a rate of 20 °C min^{-1}.

Method 3: The furnace was rapidly heated up to 1400 °C at a rate of 120 °C min^{-1}, and held at this temperature for 60 min. After the furnace had been cooled to room temperature at a rate of 20 °C min^{-1}, the products were deposited on the Si substrate over a temperature range from 950 to 1150 °C.

To demonstrate the control of the size of the CdSe/SiO_2 nanocables, four samples were prepared by Method 2, and then these were subjected to different rates of cooling. For the first sample, after the furnace temperature had been kept at 1400 °C for 60 min, the electric source was switched off and the ceramic tube with the precursors and the reaction products was cooled in air; for the other three samples, the time fixed for the furnace to be cooled to room temperature was 60, 90, and 120 min, respectively. By altering the rate of cooling, the time of re-deposition of SiO_2 was changed, and thus the thickness of the SiO_2 shell was controlled. The general morphology and chemical composition of the products were examined by field-emission scanning electron microscopy (FESEM JEOL JSM 6700F) with an energy-dispersive X-ray (EDX) spectroscope attached to the FESEM, and X-ray diffraction ((XRD) PW1710 instrument with $Cu_{K\alpha}$ radiation). Detailed microstructures of the products were further investigated by transmission electron microscopy (TEM), selected area electron diffraction (SAED), and high-resolution transmission electron microscopy ((HRTEM) JEOL 2010, operated at 200 kV). Photoluminescence (PL) spectra were recorded at room temperature with an Edinburgh luminescence spectrometer (FLS 920) using a xenon lamp (900) as the excitation source. The optical properties were also characterized by UV/Vis absorption spectroscopy.

Acknowledgements

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